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IN THE SPECIFICATION

[0020] The process requirement of the method of this invention is to insert an additional layer of dielectric material between the gate polysilicon of the gate electrode 18 and the spacers 26S for the purpose of eliminating the exposed polysilicon of the gate polysilicon of the gate electrode 18 and avoiding the formation of spurious epitaxial growth during the formation of raised source/drain regions 28S/28D.

[0021] FIG. 2A shows the device 10 of FIG. 1A, which has been modified in accordance with this invention by forming an amorphous silicon layer ~~21B~~ 21 in ~~on~~ the upper surface of the gate electrode 18 prior to forming the hard mask 22 on the top surface of the gate electrode 18, above the amorphous silicon layer 21. Then notches 24 (shown in FIGS. 3F and 3G) were formed at the top of the gate electrode 18 by etching away the outer edges of the amorphous silicon layer ~~21B~~ 21 as shown in FIGS. 3F and 3G. The notches 24 at the top of the gate electrode 18 were filled with dielectric plugs 26P thereby forming a Top Notched Gate (TNG) structure. The notches 24 were filled with the dielectric plug 26P to prevent formation of the kinds of nodules 28T seen in FIG. 1B on the polysilicon at the upper end of the gate electrode 18 as shown in FIGS. 3H and 3I.

[0026] Preparation for the selective undercut of a thin region at the top of the gate polysilicon of gate electrode 18 of FIGS. 2A and 2B must be done in a controlled and repeatable manner by forming an amorphous silicon layer 21B, FIG. 3B, in ~~on~~ the surface of the polysilicon layer 18B of FIG. 3A which is to be formed into the ~~a~~ gate electrode 18 of FIGS. 2A, 2B, 3I and 3J.

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[0028] FIG. 3B shows the stack of FIG. 3A after the first step of the present invention leading to the formation of the TNG structure of this invention, which is to form a blanket, thin amorphous silicon layer 21B ~~on~~ in the top surface of the blanket polysilicon layer 18B in the process of ion implantation of ions 21B into the top surface of the blanket polysilicon layer 18B provided for formation of the gate electrode 18. Germanium or silicon ions (21I) are implanted ~~to~~ with a dose sufficient to amorphize the desired thickness of the blanket polysilicon layer 18B. The thickness of the amorphous silicon layer 21B can be tailored by the choice of ion energy used.

[0032] FIG. 3F shows the device 10 of FIG. 3E after the TNG selective formation of the notches 24 in the amorphous silicon layer 21B of FIG. 3E as undercut notches 24 below the hard mask 22 to form an amorphous silicon cap layer 21 between the notches 24. ~~Selective undercut~~ A step of selective undercutting of the amorphized layer 21B is performed to form the amorphous silicon cap layer 21 ~~is done during~~ by a process of polysilicon RIE (described in detail below).